UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PAPPAS, PETER

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/790,953	SEILER ET AL.
	Examiner	Art Unit	
	PETER-ANTHONY PAPPAS	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _02 January 2008_.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-11,13-15,19 and 23-30_ is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) _1-11,13-15,19 and 23-30_ is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on _04 October 2006_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
        application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1-11, 13-15, 19 and 23-30 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Aila et al. (U.S. Pub. No. US 2005/0134588 A1) in view of Greene et

al. (U.S. Patent No. 5, 579, 455).

3.   In regard to claim 1 Aila et al. teaches a method and apparatus for image

processing (Abstract; p. 2, ¶ 18). When images are processed, the frame buffer

(including the color buffer and the z buffer) containing pixels of an image is typically

divided into sets of pixels often called tiles. The tiles are often non-overlapping

rectangular areas. For example, an image can be divided into non-overlapping 8x8

pixel regions (pp. 3-4, ¶ 52).

To accelerate rendering of an image, the following extra information is often

stored for each tile: the minimum of all depth values in the tile, Z-min, and the maximum

of all depth values in the tile, Z-max (e.g., tile Z-min and tile Z-max). It is appreciated

that for processing shadow information more efficiently, a new concept may be

introduced. The perimeter of the tile and the minimum and maximum depth values

define a tile volume. For a rectangular tile, for example, the tile volume is a 3D axis-

aligned box in screen space, defined by the horizontal and vertical bounds of the

rectangular tile together with the Z-min and Z-max values (p. 4, ¶ 53). It is appreciated

that the tile volume need not necessarily be defined using the minimum and maximum

depth values relating to a tile. A tile volume can be determined using the depth values

relating to a tile in a different way. An alternative is, for example, the use of two planes:

one plane in front of all depth values relating to a tile, and the other plane behind the

depth values, for instance. The planes can be determined based on the depth values

relating to the tile. The Z-min and Z-max values are, however, a very convenient way to

define the tile volume, as this information is typically available (p. 4, ¶ 53).

To further enhance the performance of the graphics processor, it is possible to

use a hierarchical stencil buffer or other hierarchical information store for shadow

information (stencil code). If the result (stencil value) of the stencil test can be

determined from a tile-specific entry of the hierarchical stencil buffer (containing a

shadow mask), the per-pixel stencil buffer entries need not be accessed (p. 6, ¶ 83; p.

7, ¶ 88; Fig. 4). It is implicitly taught that said entries are accessed. It is noted that

accessing said stencil buffer entries is considered to read on updating.

Aila et al. teaches determining whether to render a plurality of pixels within the

tile (e.g., plurality of pixels belonging to respective objects that are within the boundary

of a tile) based on depth information (p. 1, ¶ 5-6). However, Aila et al. fails to explicitly

teach a hierarchical Z value range for which to compare said previously disclosed Z

value range with. Greene et al. teaches a hierarchical Z-buffer scan-conversion

algorithm that does well on both (a) quickly rejecting most of the hidden geometry in a

mode, and (b) exploiting the spatial and temporal coherence of the images being

generated. The method uses two hierarchical data structures, an object-space octree and an image-space Z-pyramid, in order to accelerate scan conversion. The two hierarchical data structures make it possible to reject hidden geometry (hierarchical Z value test fails) very rapidly while rendering visible geometry (hierarchical Z value test passes) with the speed of scan conversion (Abstract; col. 5, lines 66-67; col. 6, lines 1-8; col. 41-67; col. 18, lines 1-8). Greene et al. teaches that for each such Z-max element, the depth value which is written into that element is the farthest depth value in any of the Z-max elements which are covered by such Z-max element in the next finer granularity level of depth buffer 502 (hierarchical Z value range). If the depth buffer 502 also includes Z-min elements, then the inner iteration also visits each of the Z-min elements in the current level. For each such Z-min element, the depth value which is written into that element is the nearest depth value in any of the Z-min elements which are covered by such Z-min element in the next finer granularity level (col. 14, lines 48-62). It is noted that a respective Z-min and Z-max (e.g., cache Z-min and cache Z-max) values for a given element [e.g., Fig. 5A element (tile) 512] are considered to represent a tile Z value range.

It would have been obvious to one skilled in the art, at the time of the Applicant's invention, to incorporate the teachings of Greene et al. into the method taught by Aila et al., because through such incorporation it would allow for quicker rejection of hidden geometry (Greene et al. – Abstract) thus improving the overall efficiency of said system. In addition Aila et al. teaches a rasterizer (e.g., rasterizer 514) for converting a polygon into pixels or samples inside the polygon (p. 5, ¶ 69). Greene et al. teaches a means of

accelerating scan conversion (Abstract). It is noted that scan conversion is considered

an element of rasterization and thus through such incorporation it would provide a

means of processing a greater amount of information in less amount of time resulting in

improved efficiency.

4.   In regard to claim 2: stencil test fails see Aila et al. – p. 7, ¶ 86; stencil test

passes see Aila et al. – p. 7, ¶ 89; and hierarchical Z value test passes see Greene et

al. – Abstract.

5.   In regard to claim 3 the rationale disclosed in the rejection of claim 2 is

incorporated herein.

6.   In regard to claim 4: stencil test fails see Aila et al. – p. 7, ¶ 86.

7.   In regard to claim 5 see Greene et al. – col. 11, lines 4-12; col. 14, lines 48-67;

col. 15, lines 1-6; col. 17, lines 24-40.

8.   In regard to claim 6 it is noted that the respective claim language fails to disclose

what exactly constitutes a "background value" or "stencil value." Aila et al. teaches the

use of a multiple-bit indicator for said stencil code ("…the shadow volume rasterization

uses only a small subset of the 8-bit stencil buffer values … a four bit stencil value is

used…" – pp. 8-9, ¶s 101-102), which specifics a relation of a plurality of stencil values

in the tile relative to a background value ("...pixels of an image … divided into sets of

pixels often called ties…" – p. 3, ¶ 52; "…the contribution of the light source is

accumulated into the frame buffer by rendering the shadow mask from the stencil

buffer…" – p. 7, ¶ 92; "…entries for storing stencil values (or, more generally, shadow

information) were discussed. It is appreciated that the tile-specific entries of a stencil

buffer (or other information store may be implemented as a combination of a Boolean

value and a stencil value..." – p. 8, ¶ 99). It is noted that a "background value" is

considered to read on shadow information which affects how a give pixel or pixels are

rendered visually. It is noted that that said claim language comprises open-ended

language (e.g., comprising) and therefore the language "wherein the stencil code is a

three bit data value" is not considered to read on "wherein the stencil code is only a

three bit data value." It is further noted that a four bit data value is considered to include

a three bit data value and therefore the respective claim limitations are considered to be

met.

9.   In regard to claim 7 the rationale disclosed in the rejection of claim 1 is

incorporated herein. Aila et al. teaches per-pixel processing (p. 5, ¶ 70). It is noted that

each of said depth elements 512 are considered to represent respective pixel elements

204 (Greene et al. – Figs. 2, 5A) and therefor result, at least in part, in per-pixel

processing.

10.   In regard to claim 8 it is noted that the respective claim language fails to disclose

what exactly constitutes a "background value" or "stencil value." The rationale disclosed

in the rejection of claims 1 and 6 are incorporated herein.

11.   In regard to claim 9 Aila et al. teaches that if the Boolean boundary value

(indicator) in the temporary tile classification buffer is TRUE for a tile, this needs to be

rasterized using a finer resolution, for example, using per-pixel resolution. Otherwise

the rasterization can be skipped, because the entire tile is either in shadow or lit (p. 7, ¶

86).

12.   In regard to claim 10 the rationale disclosed in the rejection of claim 7 is incorporated herein.

13.   In regard to claim 11 the rationale disclosed in the rejection of claim 8 is incorporated herein (Aila et al. – p. 6, ¶ 83; p. 7, ¶ 88; Fig. 8).

14.   In regard to claim 13 Greene et al. further teaches that if the Z-pyramid value is closer, we know the primitive is hidden in the quadrant. If we fail to prove that the primitive is hidden in one of the quadrants, we go to the next finer level of the pyramid for that quadrant and try again. Ultimately, we either prove that the entire polygon is hidden, or we recurse down to the finest level of the pyramid and find a pixel covered by the polygon that has a Z-value farther away than the nearest Z value in the polygon (col. 6, lines 28-36). The rationale and motivation disclosed in the rejection of claim 5 is incorporated herein.

15.   In regard to claim 14 the rationale disclosed in the rejection of claim 8 is incorporated herein. It is noted that when respective pixels of a tile are considered lit, respective to a mask, and a hierarchical Z value test passes that a positive indication is considered to be set.

16.   In regard to claim 15 the rationale disclosed in the rejection of claims 3 and 4 are incorporated herein.

17.   In regard to claim 23 the rationale disclosed in the rejection of claims 1 and 5 are incorporated herein. It is inherent that said tile, comprised of a plurality of pixels for display, has a location. It is noted a comparator (Aila et al. – Fig. 5, element 501) is considered coupled to a hierarchical Z buffer (Aila et al. – Fig. 5, element 521; Greene

et al. – Fig. 1, element 104), stencil cache (Aila et al. – Fig. 5, element 523) and

hierarchical Z buffer and stencil cache updater (Aila et al. – Fig. 5m, element 510). It is

noted that the respective claim langue is silent as to what exactly defines an

"association" between a cache MinZ and cache MaxZ and the location of the tile. It is

noted said association is considered the portion of space covered (e.g., Greene et al.)

by a respective portion of said tile or portion of said tile. As previously disclosed Alia et

al. teaches that to further enhance the performance of the graphics processor, it is

possible to use a hierarchical stencil buffer or other hierarchical information store for

shadow information (stencil code). If the result (stencil value) of the stencil test can be

determined from a tile-specific entry of the hierarchical stencil buffer (containing a

shadow mask), the per-pixel stencil buffer entries need not be accessed (p. 6, ¶ 83; p.

7, ¶ 88; Fig. 4).

18.   In regard to claim 19 the rationale disclosed in the rejection of claim 23 is

incorporated herein Aila et al. – p. 6, ¶ 83; p. 7, ¶ 88; Fig. 4).

19.   In regard to claim 24 the rationale disclosed in the rejection of claim 17 is

incorporated herein.

20.   In regard to claim 25 the rationale disclosed in the rejection of claim 22 is

incorporated herein.

21.   In regard to claim 26 the rationale disclosed in the rejection of claim 23 is

incorporated herein Aila et al. – p. 6, ¶ 83; p. 7, ¶ 88; Fig. 4).

22.   In regard to claim 27 the rationale disclosed in the rejection of claims 11 and 13

is incorporated herein.

23.   In regard to claim 28 the rationale disclosed in the rejection of claim 14 is

incorporated herein.

24.   In regard to claim 29 the rationale disclosed in the rejection of claim 1 is

incorporated herein.

25.   In regard to claim 30 the rationale and motivation disclosed in the rejection of

claim 27 is incorporated herein. Aila et al. fails to explicitly teach generating a signal

indicating that a detailed depth test is not required because all pixels of the tile are

known to be visible in the hierarchical Z plane. It is noted that the respective claim

language fails to disclose what exactly constitutes a "detailed depth test" and therefore

a "depth test" is considered to read on a "detailed depth test." Greene et al. teaches

indicating that a depth test is not required because all pixels of the tile are known to be

visible in the hierarchical Z plane (col. 6, lines 60-66; col. 7, lines 1-4).

Response to Arguments

26.   In response to Applicant's remarks that Aila et al. and Greene et al. essentially

perform the same task it is the position of the Examiner that Aila et al. and Greene et al.

share some similarities but that said similarities do not result in Aila et al. and Greene et

al. performing the exact same task or performing the exact same steps. Assuming each

Aila et al. and Greene et al. perform the exact same task and the end results are the

same, which is not the position of the Examiner, any difference in how said tasks are

performed has significance and cannot be overlooked merely because the end results

arguably are the same. For example, assuming two system perform the exact same

task such as rendering graphic information. One reference discloses a means of

accelerating scan conversion (rasterization) and the other reference discloses a

rasterization step. Would it not be advantageous to increase the efficiency of the

system with the rasterization step through the incorporation of said acceleration? The

Applicant is directed to point 27 disclosed below.

27.   In response to Applicant's remarks that there is no suggestion to combine the

references, the Examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the

references themselves or in the knowledge generally available to one of ordinary skill in

the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re

Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In light of Applicant's remarks the respective motivation has been further clarified.

It is the position of the Examiner that it would have been obvious to one skilled in the

art, at the time of the Applicant's invention, to incorporate the teachings of Greene et al.

into the method taught by Aila et al., because through such incorporation it would allow

for quicker rejection of hidden geometry (Greene et al. – Abstract) thus improving the

overall efficiency of said system. In addition Aila et al. teaches a rasterizer (e.g.,

rasterizer 514) for converting a polygon into pixels or samples inside the polygon (p. 5,

¶ 69). Greene et al. teaches a means of accelerating scan conversion (Abstract). It is

noted that scan conversion is considered an element of rasterization and thus through

such incorporation it would provide a means of processing a greater amount of

information in less amount of time resulting in improved efficiency.

28.   In response to Applicant's remarks that at no point does either reference teach, suggest or contemplate the comparison of a tile Z value range to a hierarchical Z value range the Applicant is directed to the rejection of claim 1, which has been further clarified. Greene et al. teaches the comparison of a tile Z value range to a hierarchical Z value range (col. 14, lines 48-62; Figs. 5, 5a).

29.   In response to Applicant's remarks in regard to claim 8, specifically that the cited prior art of record fails to teach "a multiple-bit indicator which specifies a relation of a plurality of stencil values in the tile relative to a background value," the Applicant is directed to the respective above rejection which has been clarified to address said remarks.

30.   Applicant's remarks have been fully considered but are not deemed persuasive.

31.   The Applicant is encouraged to schedule an interview with the Examiner to discuss the instant application if the Applicant feels it would be beneficial.

Conclusion

32.   The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: Foley et al. (pp. 870-871).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PETER-ANTHONY PAPPAS whose telephone number is (571)272-7646. The examiner can normally be reached on M-F 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

                                                    Peter-Anthony Pappas
                                                    Examiner
                                                    Art Unit 2628

/Peter-Anthony Pappas/
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